Claim 1. Amended Claim 5 recites, "a ***unitary*** insulating layer ***directly contacting and sandwiched between*** the first and second conductive elements..."

In direct contrast, Yau does not teach a unitary insulating layer directly contacting and sandiwched between conductive elements within an integrated circuit. Instead, Yau teaches the deposition of a plurality of consecutive dielectric layers between consecutive metal layers in a dual damascene structure. As is evidenced by each of the claims therein, Yau teaches forming at least three dielectric layers within his structure. In particular, he describes two dielectric layers, separated by an etch stop or "cap" layer.

In addition, Yau's specification evidences the multilayer structure of his invention:

> In a preferred embodiment, a porous silicon oxide layer is deposited on a patterned metal layer by reaction of the organo silane compound and nitrous oxide using low levels of pulsed RF power. A self-planarizing dielectric layer is then deposited in the same chamber by reaction of the organo-silane compound and a peroxide bonding compound such as hydrogen peroxide in the absence of RF power. (Column 3, lines 30-37)

Yau further characterizes his invention under a section entitled "Deposition of the Oxidized Organo Silane Dielectric in a Three-Layer Gap Filling Process." (Column 11, lines 9-10). Therein, Yau states:

> The deposition step 205 can include a capacitively coupled plasma or both an inductively and a capacitively coupled plasma in the process chamber 15 according to methods known in the art. An inert gas such as helium is commonly used in the PECVD deposition to assist in plasma generation. A gap fill layer is then deposited 210 on the liner layer by known methods. The gap fill layer is preferably self-planarizing, such as spin-on polymers or porous oxides deposited in liquid form by reaction of methyl silane and hydrogen peroxide. A cap layer is then deposited 215 on the gap fill layer, preferably using the same process for depositing the lining layer. (Column 11, lines 19-30)

Only after depositing the multi-layer structure does Yau begin the annealing process.

As reflected in the amended claims, the specification and the drawings, the unitary insulating layer of the preferred embodiment is sandwiched between and in direct contact with conductive elements within an integrated circuit. As stated on page 2 of the specification, "Advantageously, the material can be formed with a low dielectric constant without the need for a cap layer." Instead of forming a plurality of layers, as taught by Yau, the claimed invention recites the deposition of only a single layer. On page 2, the specification provides, "An

organosilane gas source is reacted with an oxidizing agent to form a layer over the substrate. The layer is predominantly formed of silicon hydroxide and incorporates carbon. This layer is then plasma treated without forming a layer during the plasma treatment. The treatment converts the silicon hydroxide layer to an insulating material having a lower dielectric constant."

Thus, Yau did not teach each and every limitation of amended independent Claims 1 and 5, and so failed to anticipate these claims. Furthermore, the dependent claims add further distinguishing features of particular utility. Accordingly, Applicant submits that all claims are allowable over Yau.

Anticipation by Maeda et al.

The Examiner has rejected Claims 1 and 2 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,800,877 to Maeda et al. ("Maeda").

Amended Claim 1 recites, "A unitary layer of insulating material directly contacting and formed between conductive elements in an integrated circuit, comprising a polysiloxane network ***consisting essentially of silicon, oxygen, carbon and hydrogen*** and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3." Claim 2 is dependent upon Claim 1 and thereby includes the limitations present in Claim 1.

As described on page 7 of the specification, the preferred method of creating the layer of insulating material includes an exemplary reaction of an organosilane gas source with an oxidizing agent is described. The reaction is of the form:

$$CH_3SiH_3 + H_2O_2 \rightarrow CH_3Si(OH)_3 + Si(OH)_4 \qquad \text{(Eq. 1)}$$

where the deposited product is predominantly $Si(OH)_4$. The reaction also produces volatile by-products such as H_2, H_2O, CO, CO_2, etc. No fluorine is described in the preferred reactants or resultant products, and the skilled artisan will readily appreciate from the disclosure as filed that the application is directed to carbon-containing oxides, rather than fluorinated compounds, for obtaining a low k material.

Maeda does not teach reacting an organosilane gas source to form a unitary layer consisting essentially of silicon, oxygen, carbon and hydrogen, as described in Claim 1. Instead, Maeda specifically teaches forming a fluorine-containing silicon oxide film using an organic silane source gas which has a Si-F bond. Organic silanes having a Si-F bond, as taught by

Maeda, include fluoroalkoxysilanes, fluoroalkylsilanes and chain fluorosiloxanes. (Col. 6, lines 37-49)

As is apparent from the patent, fluorine is an essential component of the Maeda disclosure. For example, the title of the Maeda patent is, "Method for Forming a Fluorine Containing Silicon Oxide Film." Throughout the reference, Maeda consistently refers to the film as a "fluorine-containing silicon oxide film." Furthermore, Maeda's Abstract specifically states, "In a method for forming a film by thermal CVD, a fluorine-containing silicon oxide film is formed on a substrate by thermal reaction of a mixed gas while heating the substrate. The mixed gas includes an organic silane having a Si-F bond, an organic silane having no Si-F bond, and ozone." Finally, both the specification and the claims of the Maeda reference explicitly and repeatedly refer to the "fluorine-containing silicon oxide film." Thus, it appears essential that the film disclosed by Maeda contain fluorine.

In direct contrast to the Maeda reference, amended Claim 1 excludes any substantial amount of fluorine. Claim 1 recites "a unitary layer of insulating material directly contacting and formed between conductive elements in an integrated circuit, comprising a polysiloxane network consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3." In supporting Claim 1, the specification teaches methylsilane as the preferred organosilane gas and teaches dimethylsilane and trimethylsilane as other gases the skilled artisan will recognize as reacting to form a layer predominantly of silicon hydroxide and consisting essentially of silicon, oxygen, carbon and hydrogen.

Thus, Maeda did not teach each and every limitation of amended independent Claim 1, and dependent Claim 2, and so failed to anticipate these claims. Furthermore, the dependent claims add further distinguishing features of particular utility. Accordingly, Applicant submits that all claims are allowable over Maeda.

Anticipation by Nishiyama et al.

The Examiner has rejected Claim 5 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,429,995 to Nishiyama et al. ("Nishiyama").

Amended Claim 5 recites, "a unitary insulating layer directly contacting and sandwiched between the first and second conductive elements, the insulating layer comprising polysiloxane, ***consisting essentially of silicon, oxygen, carbon and hydrogen***."

As evidenced by its title, Nishiyama is directed to a "Method of Manufacturing Silicon Oxide Film Containing Fluorine." Like Maeda, Nishiyama's disclosure repeatedly refers to the use of fluorine. For example:

> According to the present invention, there is provided a method of manufacturing a semiconductor device, in which a silicon oxide film containing fluorine, said film acting as an insulating film for electrically isolating conductive layers included in a semiconductor device, is formed by a plasma CVD method using an organic silane gas containing fluorine.
>
> The organic silane gas containing F, which is used in this method, has a Si-F bond...The organic silane gas containing F can be used singly or in combination with at least one of gases selected from the group consisting of an oxidizing gas and another gaseous compound containing F.
>
> ...The other gaseous compound containing F includes, for example, NF_3, CF_4, ClF_3, C_2F_6, SiF_4, SiH_3F, SiH_2F_2 and $SiHF_3$.

(Column 2, Lines 35-54).

In direct contrast to the Nishiyama reference, amended Claim 5 excludes any substantial amount of fluorine. As discussed previously, no fluorine is described in the preferred reactants or resultant products, and the skilled artisan will readily appreciate from the disclosure as filed that the application is directed to carbon-containing oxides, rather than fluorinated compounds.

In supporting Claim 5, the specification teaches methylsilane as the preferred organosilane gas and teaches dimethylsilane and trimethylsilane as other gases the skilled artisan will recognize as reacting to form a layer predominantly of silicon hydroxide and consisting essentially of silicon, oxygen, carbon and hydrogen.

Thus, Nishiyama did not teach each and every limitation of amended Claim 5, and so failed to anticipate this claim. Furthermore, the dependent claims add further distinguishing features of particular utility. Accordingly, Applicant submits that all claims are allowable over Nishiyama.

Claim Rejections under 35 U.S.C. §103

The Examiner has rejected Claims 4-10 under 35 U.S.C. 103 as being unpatentable over Maeda in view of U.S. Patent No. 5,869,379 to Gardner et al. ("Gardner").

As discussed above, Maeda taught dielectric constant reduction by plasma treatment ***only*** for fluorine-containing silicon oxide, and did not teach or suggest that plasma treatment would produce the same effect in any other films. The teachings of Maeda were very specific to ***fluorine-containing silicon oxide*** materials only. His motivation was to provide a stable, fluorine-containing silicon oxide film with good step coverage and a small dielectric constant. Maeda taught that plasma treatment of the fluorine-containing silicon oxide film lowered its dielectric constant, which was already low because of the fluorine content.

Gardner teaches the fabrication of a transistor in which air gaps are formed laterally adjacent the sidewall surfaces of the gate conductor.

According to the Examiner, "It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the fluorine-containing silicon dioxide taught by Maeda et al as a sidewall spacers or and [sic: an] interlevel dielectric in order to reduce capacitive coupling." (Office Action, p. 5)

Although Applicants do not address the suggestion (or lack thereof) in the art for combining the references as set forth by the Examiner, even if there were a suggestion in the art for the combination, one skilled in the art would still not have arrived at the claimed invention. As stated previously, Claims 4-10 exclude substantial levels of fluorine. Consequently, any combination that depends upon fluorine to lower the dielectric constant would not render the claimed invention obvious.

Applicant has not addressed the further rejections of dependent claims as being moot in view of the amendments and remarks herein. However, Applicant expressly does not acquiesce in the Examiner's findings not addressed herein. Indeed, Applicant submits that the dependent claims recite further distinguishing and non-obvious features of particular utility. Thus, Applicant respectfully traverses the rejections under 35 U.S.C. 103 insofar as they apply to Claims 4-10, as amended herewith, and submit that the pending claims are patentably distinct over the cited references.

CONCLUSIONS

Applicant respectfully submits that all pending claims are allowable over the art of record. Prompt allowance is earnestly solicited. If the Examiner believes that an additional telephone conference is necessary, he is invited to contact the undersigned attorney at the telephone number listed below.

The specific changes to the specification and claims are shown on a separate set of pages attached hereto and entitled **VERSION WITH MARKINGS TO SHOW CHANGES MADE**, which follow the signature page of this Response. On this set of pages, the insertions are underlined while the ~~deletions are stricken through.~~

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: Oct. 21, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as set forth below.

1. (Amended) ~~An~~ A unitary layer of insulating material directly contacting and formed between conductive elements in an integrated circuit, comprising a polysiloxane network consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3.

2. The insulating material of Claim 1, having a dielectric constant of less than about 3.2.

3. The insulating material of Claim 1, having a carbon content of between about 5% and 20% relative to a silicon content.

4. The insulating material of Claim 1, wherein the conductive elements comprise metal runners.

5. (Amended) An integrated circuit, comprising:

a first conductive element providing a first electrical path of the circuit;

a second conductive element providing a second electrical path of the circuit; and

a unitary insulating layer directly contacting and sandwiched between the first and second conductive elements, the insulating layer comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon therein and having a dielectric constant of less than about 3.5.

6. The integrated circuit of Claim 5, wherein the insulating layer has a dielectric constant of less than about 3.3.

7. The integrated circuit of Claim 6, wherein the first and second conductive elements are metal runners.

8. The integrated circuit of Claim 6, wherein the first and second conductive elements are transistor active areas within a semiconductor substrate.

9. The integrated circuit of Claim 8, wherein the insulating layer comprises a sidewall spacer.

10. The integrated circuit of Claim 9, wherein the first conductive element is a transistor gate electrode and the second conductive element is a contact to a transistor active area.

IN THE SPECIFICATION:

Please amend the specification as set forth below.

On page 14, please amend the paragraph beginning on line 8 and ending on line 14 as indicated below:

As shown in Figure 15, a second metal or metal 2 layer ~~30~~ 31 is then deposited over the low k material 16" and into the contacts 17". In accordance with current circuit density, the contact 17" is difficult to fill with standard physical vapor deposition (PVD) techniques. Accordingly, the second metal layer ~~30~~ 31 is preferably deposited by a hot metal process, such as by deposition of aluminum at greater than about 550°C. As with the dual damascene process described above, the metal deposition advantageously serves as an anneal to further lower the dielectric constant of the low k material 16".

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